THREE-LEVEL INDIRECT MATRIX CONVERTER WITH TWO SERIES Z-SOURCE NETWORKS

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Abstract*: In previous articles, the concept of series Z-source network has been extended to conventional indirect matrix converter to raise the voltage gain to unity and beyond. In this paper, this idea is modified and applied to a three-level indirect matrix converter. Two series Z-source networks are placed on the virtual dc-link between a rectifier and a neutral point clamped inverter on the positive and negative dc rails. Partial shoot-through states are used for voltage boosting. The series Z-source capacitor voltages and starting current stresses are reduced. A virtual space vector PWM method has been developed to ensure voltage boost ability of the converter. Simulation results from SABER are used to demonstrate the superiority of the proposed converter over the existing topology.*

1. INTRODUCTION

AC-AC power conversion is needed in several industrial applications including motor drives, wind energy conversion systems, ship propulsion and aerospace energy systems [1, 2]. The matrix converter (MC) is one of the most popular topologies among the available ac-ac converters because it provides high power density, sinusoidal input and output quantities, controllable input displacement factor, lengthy lifetime, and resilience under unfavourable conditions [3]. The MC topologies can be classified as direct and indirect. The direct MC (DMC) implements single stage ac-ac conversion, but the indirect MC (IMC) performs ac-dc-ac conversion with no intermediate dc-link capacitor. Both of them have the same behaviour, but the latter has simpler commutation than the former [4, 5], and the number

of controllable switches was reduced in sparse and ultrasparse IMCs [6]. The three-level IMC (3LIMC) is a relatively new topology from the IMC family that incorporates a three-level voltage source inverter (VSI) with the matrix converter concept [7]. The topology produces multilevel output voltages with better harmonic content compared to the two-level topology while still maintaining all the advantages outlined for the traditional IMC.

Despite all the attractive features of the MC, its penetration in industry is low compared to existing topologies [8]. This is due to the fact that MCs have two main shortcomings: 1) the voltage gain cannot exceed 0.866; and 2) the output voltage is affected by changes in the input voltage [9, 10]. The output voltage sensitivity drawback can be overcome in a limited range through improved modulation methods [11]. Many over-modulation techniques have been suggested to improve the voltage gain, however they are inadequate and often implemented at the expense of degrading the input current and output voltage quality [12]. A transformer connected between the supply and load could increase the voltage gain but this will impact on the compactness of the MC [13]. Alternatively, when an AC-boost chopper is combined with IMC the voltage gain can increase, but requires more active switches [14].

The Z-source (ZS) network offers a clever boost ability for IMC. In [8], an IMC incorporating a ZS network at the fictitious dc-link to increase the voltage gain was presented. A three-level version of the converter proposed in [8] was presented in [15, 16]. This topology is called three-level cascaded Z-source IMC (3LCZSIMC) in this paper and shown in *fig. 1*.

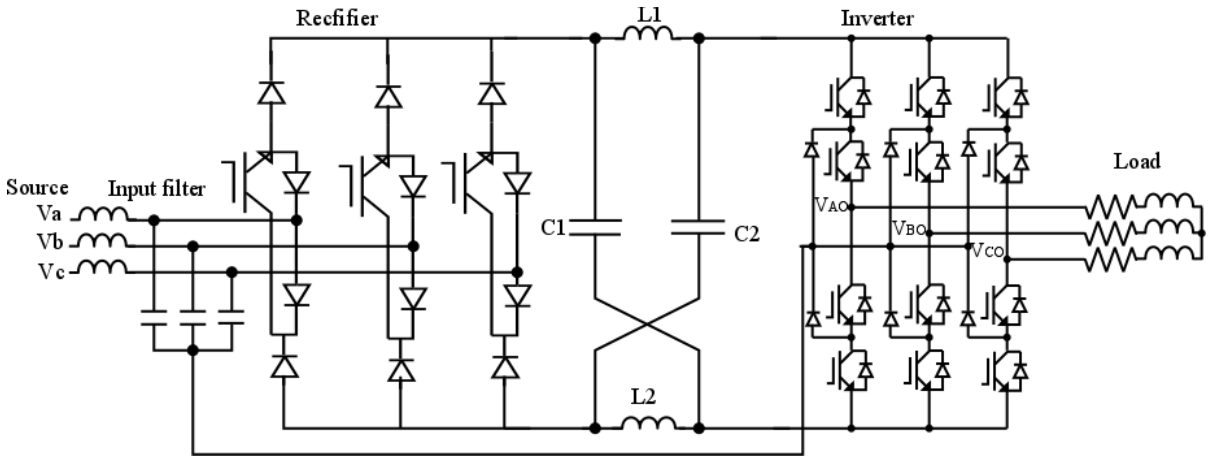


Fig. 1. Three-level cascaded Z-source indirect matrix converter

This converter brings on board the added benefits of multilevel converters such as better harmonic performance of the output waveforms and the use of low-voltage devices for applications that require medium voltage. Nevertheless, there are two weaknesses for this converter. The first issue is that the Z-source capacitor voltages are larger than the supply voltage which means larger capacitors will have to be used thereby increasing the

overall cost and volume. The other drawback is that the Z-source converter cannot suppress the inrush current and resonance between the Z-source capacitors and inductors. This causes voltage and current surges and may destroy the devices [17].

A replacement of the cascaded ZS (CZS) network proposed earlier in [8] with a series ZS (SZS) network was proposed in [18]. This circuit topology brings onboard other advantages over the cascaded topology. These include lower voltage stress on the capacitors and a reduction of the inrush current during start up. A comparison of this new topology with existing topologies for wind power application was given in [19]. In order to enhance the output harmonic performance of the converter proposed in [18], a three-level series ZS IMC (3LSZSIMC) is proposed in this work. Two series Z-source networks are inserted at the positive and negative dc rails of the three-level IMC. A virtual space vector pulse width modulation method is employed to achieve voltage-boost ability for this converter.

The rest of the paper is organized as follows. Following the introduction, the topology of the 3LSZS IMC including its operating principles and governing equations is presented in section 2; section 3 presents the modulation scheme for the converter in detail; in section 4 the criteria for selection of the series Z-source components is established; section 5 presents numerical simulations to verify the theoretical concepts; also performance comparisons with the 3LCZSIMC is given; section 6 draws the final conclusion.

2. STRUCTURE AND PRINCIPLE OF OPERATION

2.1. Structure

Figure 2 shows the topology of the proposed three-level series Z-source indirect matrix converter based on ultra-sparse IMC topology.

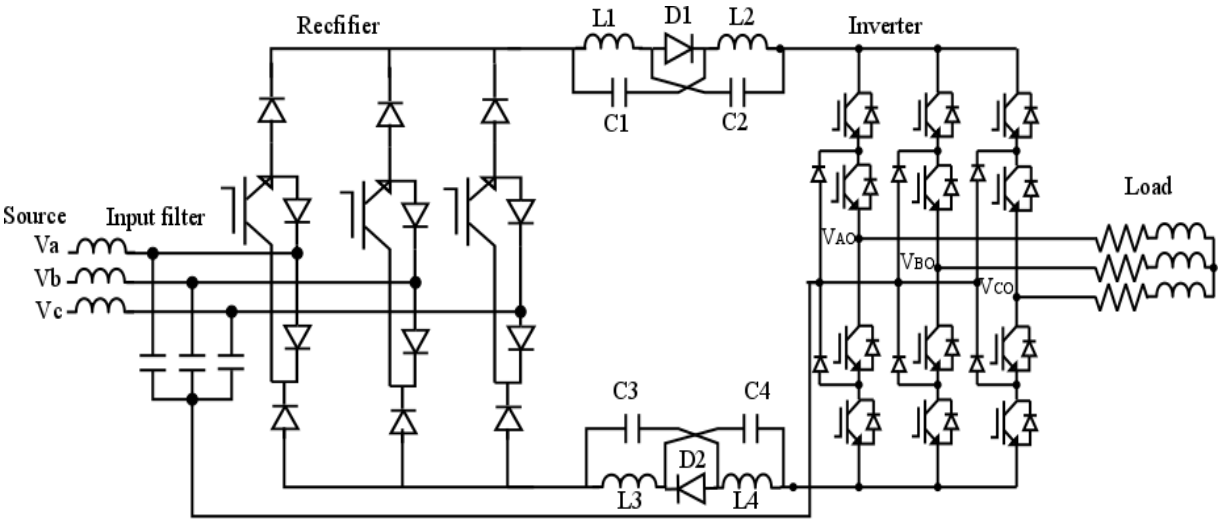


Fig. 2. Three-level series Z-source indirect matrix converter

As already stated, traditional IMCs have a drawback of limited voltage gain. To deal with this limitation, several control procedures and circuit configurations have been proposed. Specifically, the voltage gain can be increased to unity and beyond by employing Z-source network [20]. The basic function of traditional IMCs is commonly achieved in a two-stage power conversion, the first stage being ac-dc and the second dc-ac. The input stage is a current source rectifier (CSR) while the output stage is a conventional NPC inverter. Series Z-source networks are placed at the fictitious dc-link to give it voltage boost capability.

2.2. Operation

This converter is operated by employing shoot-through states as well as active and zero states used in conventional three-level IMCs. The series Z-source networks give this converter its voltage boosting ability. The capacitor voltage stress is reduced and the starting current is limited by the series Z-source networks. All these benefits are achieved while maintaining the same boost ratio of the cascaded Z-source network. Equivalent circuits of 3LSZSIMC under different states are shown in *fig. 3*.

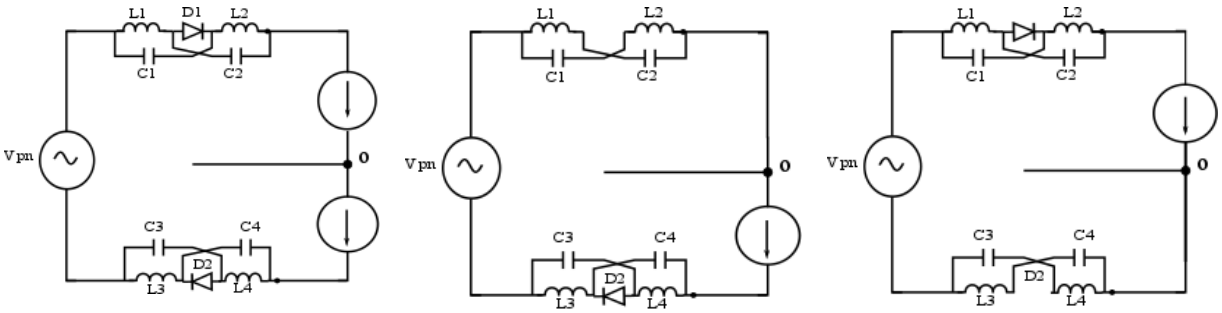


Fig. 3. Equivalent circuits of 3LSZSIMC. (a) NST states, (b) UST states, (c) LST states

For symmetry, inductances of same values and capacitances of same values are used. Thus,

$$V_C = V_{C1} = V_{C2} = V_{C3} = V_{C4} \tag{1}$$

$$V_L = V_{L1} = V_{L2} = V_{L3} = V_{L4} \tag{2}$$

Without loss of generality, the voltage across L1 is used to derive the average capacitor voltages. In the upper-shoot-through (UST) states, the positive terminal of the inverter side is shorted with the neutral point, and the inductor voltages are given by:

$$V_{L1} = V_{po} + V_{C2},\ V_{L2} = V_{po} + V_{C1} \tag{3}$$

$$V_{L3} = -V_{C3},\ V_{L4} = -V_{C4} \tag{4}$$

Similarly, during lower-shoot-through (LST) states, the negative terminal of the inverter is shorted with the neutral point, and the inductor voltages are given by:

$$V_{L1} = -V_{C1},\ V_{L2} = -V_{C2} \tag{5}$$

$$V_{L3} = V_{on} + V_{C4},\ V_{L4} = V_{on} + V_{C3} \tag{6}$$

In (3) and (6), V_{po} and V_{on} represent the upper and lower halves of the virtual dc link voltage with respect to the inverter neutral point (NP). The summation of the two terms gives the total dc-link voltage (V_{pn}).

Inductor voltages during non-shoot-through (NST) states are:

$$V_{L1} = -V_{C1} \tag{7}$$

$$V_{L2} = -V_{C2} \tag{8}$$

$$V_{L3} = -V_{C3} \tag{9}$$

$$V_{L4} = -V_{C4} \tag{10}$$

Averaging the inductor voltages (using V_{L1} in this case) over a switching period yields:

$$d_{sh-u} * T_{sw} * (V_{po} + V_{C1}) + d_{sh-l} * T_{sw} * (-V_{C1}) + (-V_{C1}) * [1 - (d_{sh-u} + d_{sh-l})] * T_{sw} = 0 \tag{11}$$

where T_{sw} is the switching period, $d_{sh\text{-}u}$ is the duty ratio of UST states while $d_{sh\text{-}l}$ is the duty ratio of the LST states. For symmetric operation, $d_{sh\text{-}u}$ is made equal to $d_{sh\text{-}l}$. The sum of the two terms is d_{st}. It should also be noted that the average values of V_{po} and V_{on} are equal and their sum equals V_{pn}. Therefore

$$V_C = \frac{d_{st}}{1-d_{st}}\left(\frac{V_{pn}}{4}\right) \tag{12}$$

It is clear from (12) that, for the 3LSZSIMC the Z-source capacitor voltages are zero for zero shoot-through duration. For soft starting, V_c can rise from zero slowly; so if we control d_{st} for it to rise gradually from zero then soft-start is realized. This is not so in a 3LCZSIMC.

In the non-shoot-through state, we can write

$$V_{dc-link} = V_{pn} + 2V_C - 2V_L \tag{13}$$

In (13), $V_{dc\text{-}link}$ denotes the output voltage of the series ZS networks which will be the input for the inverter. The boost factor, *B*, is found using (7), (12) and (13) as follows:

$$V_{dc-link} = \frac{1}{1-d_{st}} V_{pn} = BV_{pn} \tag{14}$$

where

$$B = 1/(1 - d_{st}) \tag{15}$$

The fundamental component of the output line-to-line voltage is given by

$$\hat{V}_{out} = m_i B V_{pn} \tag{16}$$

where m_i represents the modulation index of the inverter.

If we neglect power losses in the rectifier, then the input power equals the output power of the rectifier. Thus,

$$\mathrm{V_{pn}I_{pn}} = 3\mathrm{V_{in}I_{in}}\cos\theta_\mathrm{i} = \frac{3}{2}\hat{\mathrm{V}}_\mathrm{in}\hat{\mathrm{I}}_\mathrm{in}\cos\theta_\mathrm{i} \tag{17}$$

Here, I_{pn} is the current in the output of the rectifier; V_{in} is the fundamental component of the supply phase voltage; I_{in} is the fundamental component of the input current; θ_i is input current displacement angle. To get a power factor of unity, θ_i is set to zero. The input stage is a CSR which modulates the source current with modulation index m_r given by:

$$m_r = \frac{\hat{I}_{in}}{I_{pn}} \tag{18}$$

Using (17) and (18), we have

$$V_{pn} = \frac{3}{2} m_r \hat{V}_{in} \cos\theta_i \tag{19}$$

Putting (19) in (16) yields

$$\hat{V}_{out} = \frac{3}{2} m_r m_i B \hat{V}_{in} \cos\theta_i \tag{20}$$

Equation (20) defines the relationship between output and input voltages of 3LSZSIMC. It should be noted that the d_{st} must be lower than m_i; therefore, to get maximum boosting, it is assumed that

$$m_r = 1, \qquad d_{st} = 1 - m_i \qquad \theta_i = 0. \tag{21}$$

3. MODULATION TECHNIQUE

Modulation of the proposed converter is divided into CSR and voltage source inverter (VSI) modulation, respectively. The CSR has nine possible switching states with six producing non-zero currents in the dc-link. The vector diagram of the CSR is shown in *fig. 4* comprising six sectors. The current reference vector's location within a sector is identified and synthesized by two framing vectors and a null vector.

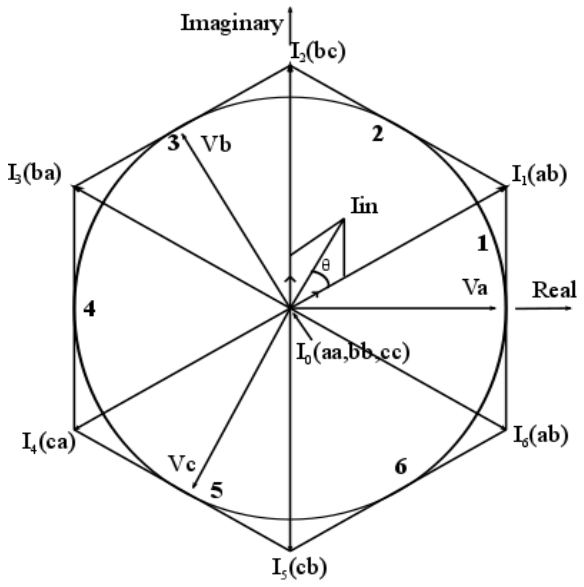


Fig. 4. Space vector diagram of rectification stage

Let angle of current reference vector be θ_r, then duty ratios of active and null vectors are calculated as follows:

$$d_\gamma = m_r \sin\left(\pi/3 - \theta_r\right) \tag{22}$$

$$d_\delta = m_r \sin(\theta_r) \tag{23}$$

$$d_{0r} = 1 - (d_\gamma + d_\delta). \tag{24}$$

The output currents circulate through the inversion stage when the output voltage is zero thereby making dc-link current delivered by the CSR zero. We can take advantage of this and make the CSR switching coincide with the instant when the inverter output voltage is zero so as to produce zero current commutation. This reduces the switching losses in the CSR [6, 21] and is achieved by eliminating completely the zero current vector and adjusting the CSR duty ratios as follows:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta},\ d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{25}$$

The back-end inverter is based on three-level NPC inverter controlled using a three-level space vector PWM technique. *Fig. 5* shows the vector diagram of a conventional NPC inverter controlled with conventional three-level space vector PWM. The diagram contains six sectors with twenty-seven switching states. The switching states can be grouped as zero, small, medium and large vectors. The letter 'P', 'O' and 'N' imply two top, middle and bottom switches, respectively, of a phase leg are turned on. In an "O" state, the input capacitors of the NPC inverter formed by the input filter capacitors become charged or discharged depending on the NP current direction. For the capacitors to have equal voltages on them, the NP current should be zero over a switching period. A conventional three-level space vector PWM cannot achieve this since it tries to use currents of small vectors to compensate those of medium vectors. This usually happens when the power factor is low and the modulation index is high.

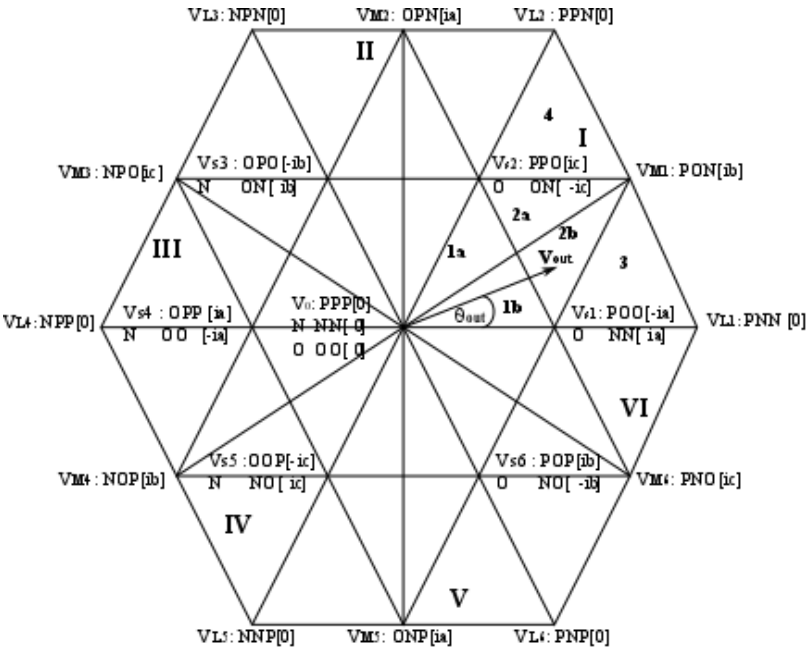


Fig. 5. Space vector diagram of inversion stage

A virtual space vector PWM technique is used to overcome this drawback. In this modulation scheme, virtual vectors are formed from existing vectors so that the average NP current is zero in a switching period. The reference voltage is then created with three nearest virtual vectors. In sector I of *fig. 5*, the virtual vectors produced are shown in *fig. 6*.

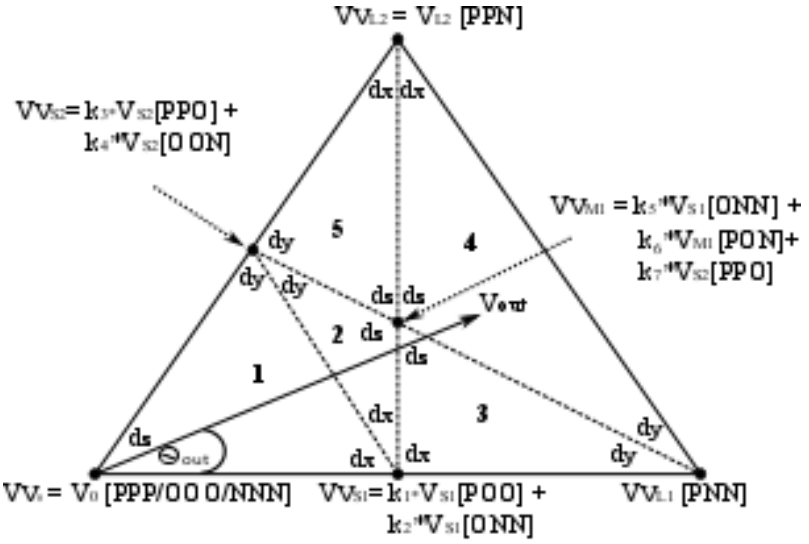


Fig. 6. Virtual space vectors for sector I

The duty ratios of the identified virtual vectors are calculated as follows:

$$d_x.V_{V1} + d_y.V_{V2} + d_z.V_{V3} = \vec{V}_{out} \tag{26}$$

$$d_x + d_y + d_z = 1 \tag{27}$$

The duty ratios of switching states making the virtual vectors are then determined. Consider triangle 3 in *fig. 6* for example. The duty ratio of the selected virtual vectors are given by:

$$d_x = 2 - m_i\left[\sqrt{3}\,\cos(\theta_{out}) + 3\sin(\theta_{out})\right] \tag{28}$$

$$d_y = \sqrt{3}m_i\cos(\theta_{out}) - 1 \tag{29}$$

$$d_z = 3\sqrt{3}m_i\sin(\theta_{out}) \tag{30}$$

In (28) to (30), m_i is the modulation index of the VSI and is defined as:

$$m_i = \frac{\sqrt{3}|\vec{V}_{out}|}{V_{pn,avg}} \tag{31}$$

The CSR and VSI stages are synchronized to ensure balance of input currents and output voltages within a switching period. For instance with the reference vector of the CSR in sector 2 and that of the VSI in triangle 4 of sector I, we have the vectors: I_1 (ac), I_2 (bc) and V_{VM1}, V_{VL1}, V_{VL2}. The virtual vectors are made from V_{S1} (ONN), V_{S2} (PPO), V_{M1} (PON), V_{L1} (PNN) and V_{L2} (PPN). The selected vectors are then applied to the input and output stages according to the switching pattern I_1 (ac) → I_2 (bc) for the CSR and PPO → PPN → PON → PNN → ONN for the VSI.

Partial shoot-through states are applied to phase legs of the VSI to achieve voltage boost operation. The resulting modified switching sequence in the output stage becomes PPO → PPL → PPN → PON → PNN → UNN → ONN with U and L representing UST and LST states, respectively. In an UST state, three top switches in a phase leg are turned on whereas in a LST state three bottom switches in a phase leg are gated on. *Figure 7* shows the switching pattern of the converter where the vectors in the VSI stage are organized in a two-sided sequence so that each side corresponds to an active vector of the CSR stage.

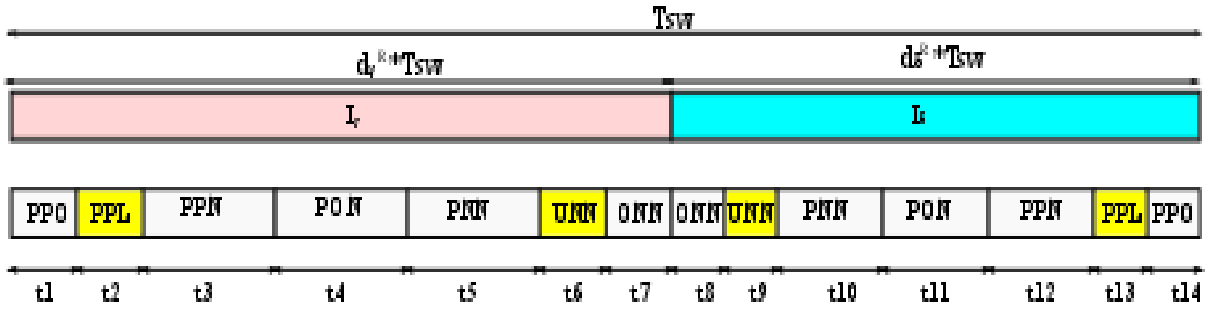


Fig. 7. Switching sequence. Top: CSR stage; Bottom: VSI stage

4. SELECTION OF SERIES Z-SOURCE PASSIVE COMPONENTS

From the analysis in section 2, the average current through the inductors is equal to that of the rectifier dc-link current in steady stste. Thus, the average current through the inductors is given by:

$$I_L = \frac{P_{out}}{V_{pn}} = \frac{P_{out}}{1.5\hat{V}_{in}\cos\theta_i} \tag{32}$$

where P_{out} represents the output power of the converter.

The series Z-source capacitor values are selected based on the desired voltage ripple and capacitor current. During the upper-shoot-through and lower-shoot-through states, as shown in *figures 3(b)* and *3(c)*, the series Z-source inductor current flows through the

capacitors and discharges them; hence, the voltage ripple across the capacitors can be expressed as:

$$\Delta V_c = \frac{I_L}{C} \cdot d_{st} \cdot T_{sw} \cdot \tag{33}$$

With ΔV_c selected to satisfy $\Delta V_c \leq k_v\%V_c$, then

$$C \geq \frac{0.5 \cdot d_{st} T_{sw}}{k_v\%V_c} I_L = \frac{2 \cdot (1-d_{st}) \cdot T_{sw}}{k_v\%V_{pn}} I_L. \tag{34}$$

Putting (32) into (34) yields:

$$C \geq \frac{(1-d_{st})T_{sw}}{1.125 \cdot k_v\% \cdot \hat{V}_{in}{}^2 \cos^2\theta_i} P_{out}. \tag{35}$$

Similarly, the series Z-source inductor values are selected based on a specified current ripple. During the NST states, as shown in *fig. 3(a)*, the series Z-source inductor current decreases, and the inductor voltage equals the capacitor voltage; therefore, the inductor current ripple can be expressed as:

$$\Delta I_L = \frac{V_C}{L} \cdot (1 - d_{st}) \cdot T_{sw} \tag{36}$$

With ΔI_L selected to satisfy $\Delta I_L \leq k_i\%I_L$, then

$$L \geq \frac{(1-d_{st})T_{sw}}{k_i\%I_L} V_C = \frac{d_{st} \cdot T_{sw}}{k_v\%I_L} V_{pn}. \tag{37}$$

Putting (19) and (32) into (37) yields

$$L \geq 0.5625 \frac{d_{st} T_{sw}}{k_i\%P_{out}} \hat{V}_{in}{}^2 \cos^2\theta_i. \tag{38}$$

5. RESULTS AND DISCUSSION

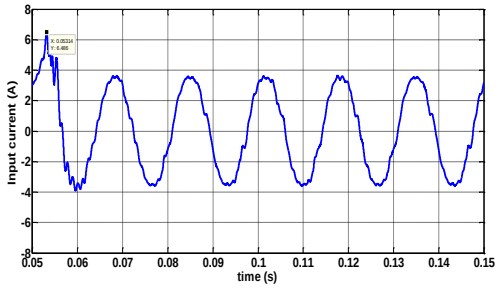
The simulations of the proposed 3LSZSIMC topology and the existing 3LCZSIMC topology are performed under the same conditions using Saber software to compare their performance. In the simulations, the converters are fed by a 122-V, 50 Hz three-phase source and supply a three-phase R-L load. For both topologies, the voltage modulation

index is set to 0.85 and the shoot-through ratio set to 0.15. A switching frequency of 10 kHz is used. A summary of the parameters used for the simulation is given in Table I.

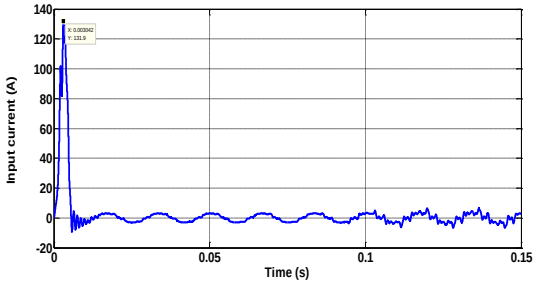
Table I. Parameters used for simulation

Description	**Value**
Input AC voltage	122 V / 50 Hz
Output frequency	100 Hz
Input filter, L and C	0.1 mH and 100 μF
Load, R-L	50 Ω , 10 mH
Series Z-source, L-C	1 mH , 1000 μF
Z-source, L-C	1 mH , 1000 μF
Switching frequency	10 kHz

Figures 8 and *9* show the simulation results for the proposed 3LSZSIMC and the existing 3LCZSIMC respectively.



(a)



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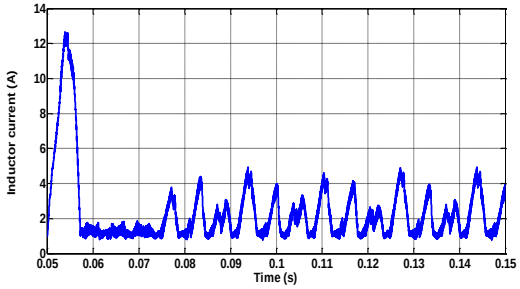

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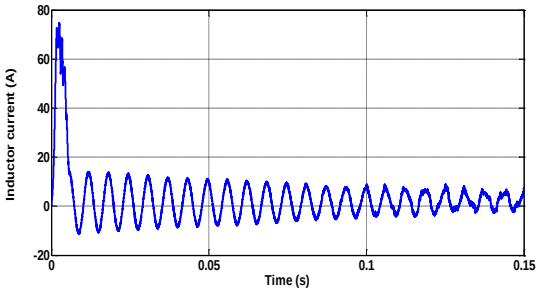

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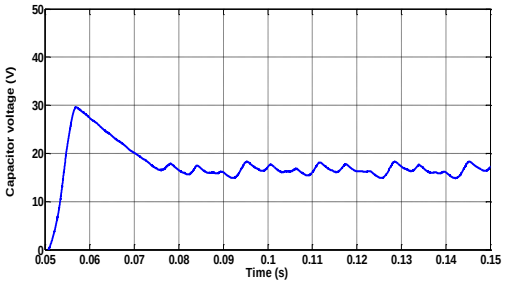

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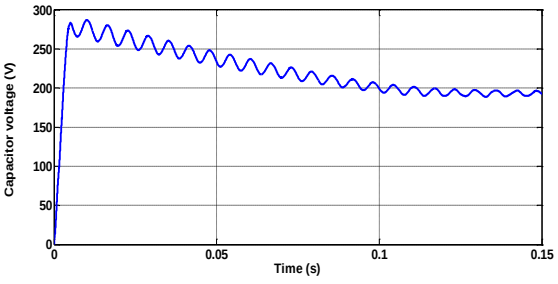

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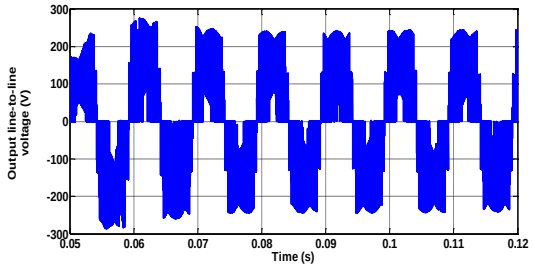
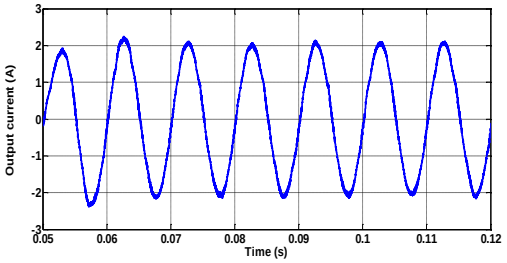
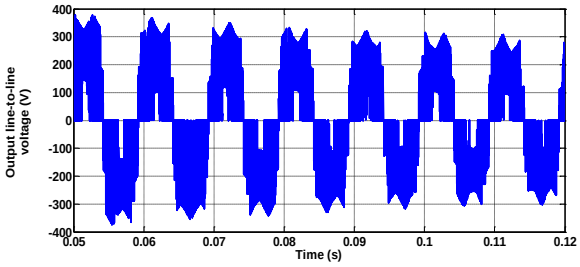


(d)



(e)

Fig. 8: 3LSZSIMC. (a) Input phase current. (b) Series Z-source inductor current. (c) Series Z-source capacitor voltage (d) Output line-line voltage. (e) Output phase current.



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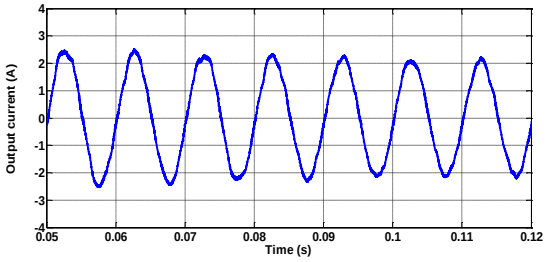

(e)

Fig. 9: 3LCZSIMC. (a) Input phase current. (b) Series Z-source inductor current. (c) Series Z-source capacitor voltage (d) Output line-line voltage. (e) Output phase current.

The simulated results for the two topologies show the soundness of the adopted modulation strategy in terms of output voltage and current waveforms. At start up, the input current drawn by the 3LSZSIMC reaches 6.5 A (see *fig. 8a*) whereas the corresponding value for the 3LCZSIMC is 132 A (see *fig. 9a*). This clearly shows that the inrush current at start up is suppressed in the 3LSZSIMC. The inductor current for the proposed series topology, 3LSZSIMC, reaches 12.7 A as shown in *fig. 8b* whereas the inductor current of the cascaded topology, 3LCZSIMC, reaches 74.7 A (see *fig. 9b*). This means that inductors of reduced sizes can be employed in the proposed topology even though four inductors are required as opposed to two in the cascaded topology.

The voltages across the Z-source capacitors are shown in *fig. 8c* and *fig. 9c*, respectively, for the two topologies. The average Z-source capacitor voltage is 16 V for the 3LSZSIMC and 195 V for the 3LCSZSIMC. The waveforms also show that the Z-source capacitors in 3LSZSIMC and 3LCZSIMC topologies have to withstand at start up peak voltages of about 30 V and 300 V respectively. Therefore, smaller sizes of capacitors can be employed in the proposed converter. Even though four capacitors are required in the proposed topology as opposed to two in the existing one, the smaller sizes of the capacitors mean light weight film capacitors could be used thereby reducing the size and overall volume of the converter.

As shown in *figures 8d* and *9d*, both converters are able to perform voltage boost by employing partial shoot-through states in the inverter state switching sequences. However, a

critical look of the two waveforms shows that the 3LSZSIMC maintains the shape of the traditional 3-level IMC waveforms even when shoot-through states are inserted whiles that of the 3LCZSIMC have some voltage spikes resulting from the extremely high Z-source capacitor voltages of the 3LCZSIMC. The output current waveforms of the two converters, shown in *figures 8e* and *9e*, are all sinusoidal. However, that of the 3LSZSIMC present better output performance in terms of total harmonic distortion (THD).

The above simulation results clearly show that the 3LSZSIMC topology presents better performance in terms of output current THD, and reduced voltage and current stresses on Z-source components and consequently reduced sizes of these components.

6. CONCLUSIONS

The ac-to-ac converter presented in this paper is a three-level indirect matrix converter having two series Z-source networks inserted in the dc link to give it voltage-boost capability. This converter topology would be suitable for applications requiring unidirectional power flow with lower output waveform harmonic content. Where bidirectional power flow is required, it can be achieved by replacing the ultrasparse rectifier with a sparse matrix rectifier. The proposed 3LSZSIMC and existing 3LCZSIMC topologies were simulated and compared in order to determine the suitability of the proposed 3LSZSIMC for applications requiring ac-to-ac power conversion such as wind energy conversion systems (WECSs). The simulation results confirm the voltage-boost ability of the proposed converter. This feature is necessary in WECSs where the generator voltage needs to be boosted so the output voltage could meet the grid requirements. The quality of the output current waveform of the proposed 3LSZSIMC was found to be better than that of the 3LCZSIMC. In addition, the Z-source capacitor voltages and inductor currents of the proposed converter are lower at start up. Therefore, the proposed converter just like the existing 3LCZSIMC is a potential candidate for WECSs.

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