MODELING AND ELECTRICAL CHARACTERIZATION OF MOSFETs 'EKV MODEL' USING MATLAB

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Abstract*: The miniaturization of MOS transistors has increased the integration density and speed of operation of the circuits. This miniaturization has led to parasitic phenomena that degrade the current-voltage characteristics. The EKV MOSFET Model resolves this problem, this component enables to progress in miniaturization. This paper presents a simulation of MOSFET 'EKV model' using Matlab to identify the different output and transfer characteristics, transconductance g_m, Methodology g_m/I_D, etc.*

1. INTRODUCTION

The reduction of the metal–oxide–semiconductor field-effect transistor (MOSFETs) sizes is accompanied by the reduction of the gate oxide thickness; different scaling limits for MOSFETs have been discussed [1, 2, 3, 4, 5]. In this context, it must have a model which is continuous in all regime of operation: weak or strong inversion. In 1995, Enz, Krummenacher and Vittoz proposed a mathematical model of metal-oxide semiconductor field-effect transistors (MOSFET) valid in all regions of operation: weak, moderate, and strong inversion so called EKV model [6] which is intended for circuit simulation and analog circuit design.

This paper describes the electrical characterization and modeling for the EKV MOSFETs model using MATLAB.

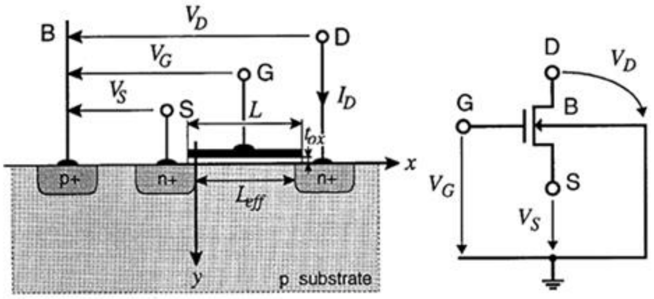

Fig. 1. Cross-section of an idealized n-channel MOS transistor and the corresponding symbol [7].

2. CONTINUOUS MODEL 'EKV MODEL'

The simulation of analog circuit, it is essential to dispose a model which is continuous in all regime of operation (weak, moderate and strong inversion). An EKV model developed in work of Enz, Krummenacher and Vittoz (the so-called "EKV model") solves the problem; EKV calculated the drain current as the combination of a forward current controlled by the source, and a reverse current controlled by the drain. All terminal voltages are called to the local substrate; therefore the inherent device symmetry is conserved. The EKV Mosfet Model is a mathematical model of metal-oxide semiconductor field-effect transistors (MOSFET) which is intended for circuit simulation and analog circuit design.

The following figure presents the log I_D–V_{GS} characteristics of a standard MOSFET.

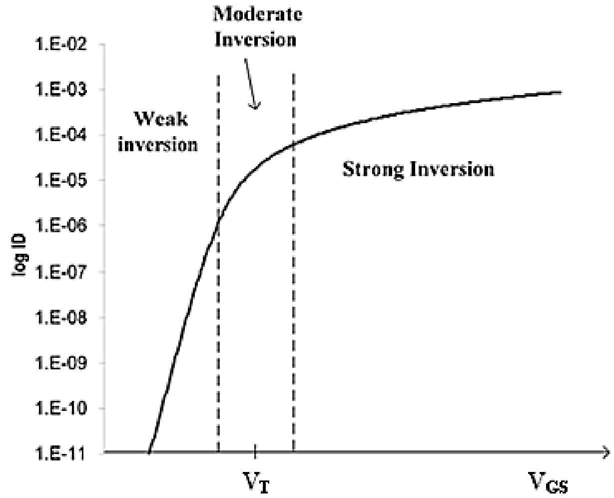

Fig. 2. Discontinuity of the I_{DS} (V_{GS}) characteristics at $V_{GS} \cong V_T$.

Their basic equation for drain current (in saturation) is given by [7,8,9,10] :

$$i = q^2 + q \ \Rightarrow i = \frac{I_D}{I_S} \Rightarrow I_D = i.I_S \tag{1}$$

$$I_S = 2nU_T^2\mu_n C_{ox}\frac{W}{L} \tag{2}$$

With $U_T = (KT/q)$

The pinch-off voltage V_P is a positive number defined as the value of the channel potential for which the inversion charge is zero in a non-equilibrium state. V_P depends on the gate voltage V_G and represents the voltage applied to the channel to equilibrate the effect of V_G. V_P is related to V_G and V_{TO} by:

$$\frac{V_P - V}{U_T} = 2(q-1) + log(q) \tag{3}$$

$$\Rightarrow q = invq\left(\frac{V_P - V}{U_T}\right) \Rightarrow V_P = \frac{(V_{GS} - V_{TO})}{n} \tag{4}$$

$$V_P = \frac{(V_{GS} - V_{TO})}{n} \;\; \Rightarrow \;\; V_{GS} = n.V_P + V_{TO} \tag{5}$$

The following figure presents the Inversion charge density vs. channel voltage.

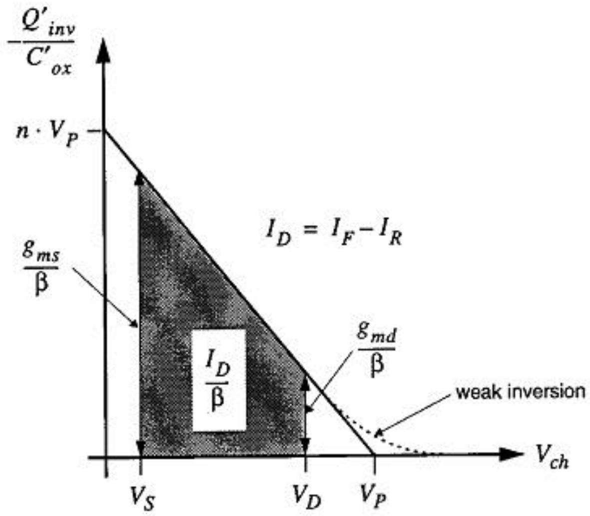

Fig. 3. The Inversion charges density vs. channel voltage.

$$I_D = \overbrace{\beta.\int_{V_S}^{\infty}\left[-\frac{Q'_{inv}(V_{ch})}{C_{ox}}\right].dV_{ch}}^{=I_F\ forward\ current} - \underbrace{\beta.\int_{V_D}^{\infty}\left[-\frac{Q'_{inv}(V_{ch})}{C_{ox}}\right].dV_{ch}}_{=I_R\ reverse\ current} \tag{6}$$

$$I_D = I_F - I_R \tag{7}$$

$$I_D = 2n\mu_n C_{ox} \frac{W}{L}\left(\frac{KT}{q}\right)^2 \left[\left\{ln\left[1 + exp\left(\frac{V_P - V_S}{\frac{2KT}{q}}\right)\right]\right\}^2 - \left\{ln\left[1 + exp\left(\frac{V_P - V_{DS}}{\frac{2KT}{q}}\right)\right]\right\}^2\right] \quad (8)$$

On the other hand, $V_S = 0$, $V_{DS} < V_P$ and $V_{GS} > V_T$ (*i.e.* the transistor is operating in the non-saturated regime). In that case the exponential terms are much larger than unity, and one can write:

$$I_D = 2n\mu_n C_{ox} \frac{W}{L}\left(\frac{KT}{q}\right)^2 \left[\left(\frac{V_P}{\frac{2KT}{q}}\right)^2 - \left(\frac{V_P - V_{DS}}{\frac{2KT}{q}}\right)^2\right] \quad (9)$$

$$I_D = \frac{1}{2} n\mu_n C_{ox} \frac{W}{L}[2V_{DS}V_P - V_{DS}^2] \quad (10)$$

$$I_D = \frac{1}{2} n\mu_n C_{ox} \frac{W}{L}\left[2\frac{(V_{GS} - V_T)V_{DS}}{n} - V_{DS}^2\right] \quad (11)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2} nV_{DS}^2\right] \quad (12)$$

With

i: normalized drain current

I_S: specific current

I_F: forward normalized current

I_R: reverse normalized current

V_P: pinch-off voltage

U_T: thermal voltage

We will now study the transconductance *gm* of this model. Transconductance is the most important parameter for MOSFETs. The equation for *gm* is given by:

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \quad (13)$$

Transconductance *gm* (in strong inversion) is given by:

$$g_m \equiv \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (14)$$

Transconductance *gm* (in weak inversion) is:

$$g_m \equiv \frac{I_D}{nU_T} \tag{15}$$

Table 1. Main EKV intrinsic model parameters for first and second order effects and defaults values and units where applicable [15,16].

Name	*Description*	*Units*
COX	*Gate oxide capacitance*	F/m^2
VTO	*Nominal threshold voltage*	*V*
GAMMA	*Body effect factor*	$V^{1/2}$
PHI	*Bulk Fermi potential(2x)*	*V*
KP	*Transconductance parameter*	A/V^2
THETA	*Mobility reduction coefficient*	*1/V*
UCRIT	*Longitudinal critical field*	*V/m*
XJ	*Source & drain junction depth*	*m*
DL	*Channel length correction*	*m*
DW	*Channel width correction*	*m*
LAMBDA	*Depletion length coefficient*	-
LETA	*Short channel effect coefficient*	-
WETA	*Narrow width effect coefficient*	-

Table 2. extraction procedure for the EKV model, sequence specifying device sizes, state (SI: strong, MI: moderate, WI: weak inversion, co.: conduction, sat.: saturation) and extracted parameters.

Device sizes	*Characteristics*	*Conditions*	*parameters*
Parameter Extraction			
Matrix W/L	I_D vs. V_G *gm* vs V_G	*WI*	*DL, DW*
Wide/long	I_D vs. V_S V_P vs. V_G I_D vs. V_G	*SI sat.* *MI sat.* *SI sat.@*V_S	I_S *VTO, GAMMA, PHI* *KP, THETA*
Wide/short	I_D vs. V_S V_P vs. V_G I_D vs. V_D	*SI sat.* *MI sat.* *SI co.-sat.*	I_S *LETA* *UCRIT, LAMBDA*
Narrow/long	I_D vs. V_S V_P vs. V_G	*SI sat.* *MI sat.*	I_S *WETA*

Table 3. Summary of basic DC simulation model equations [15,16].

Description	*Equation*
Pinch-off voltages	$V_P = V'_G - PHI - \gamma'.(\sqrt{V'_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2})$ $V'_G = V_G - VTo + PHI + GAMMA.\sqrt{PHI}$
Slope factor	$n = 1 + \frac{GAMMA}{\sqrt{V_P + PHI}}$
Transconductance, mobility reduction	$\beta = KP.\frac{W_{eff}}{L_{eq}}.\frac{1}{1 + THETA.V_P}$
Effective length & width	$L_{eff} = L + DL, W_{eff} = L + DW$
Channel length modulation & velocity saturation	$L_{eq} = L_{eff} - \Delta L + \frac{V'_{DS}}{UCRIT}$ $\Delta L = LAMBDA.L_C.In(1 + \frac{V_R}{L_C.UCRIT})$ $L_C = \sqrt{\frac{\varepsilon_0 \varepsilon_{si}}{COX}.XJ}$ $V_D - V_S \leq V'_{DS} \leq V_{DSS}$ $0 \leq V_R < V_D - V_S - V'_{DSS}$ *V'_{DS} and $V_R$are continuous functions, V_{DSS} and V'_{DSS} depend on bias, L_{eff}, UCRIT and LAMBDA*
Short & narrow channel effects	$\gamma' = GAMMA - \frac{\varepsilon_0 \varepsilon_{si}}{COX}.\left[\frac{LETA}{L + DL}.\sqrt{V_D + PHI} + \left(\frac{LETA}{L + DL} - \frac{3.WETA}{W + DW}\right).\sqrt{V_S + PHI}\right]$
Drain current and specific current	$I_D = I_F - I_R$ $I_{F(R)} = \begin{cases} I_S.exp\left[(V_P - V_{S(D)})/U_T\right] \ (WI) \\ I_S.\left[(V_P - V_{S(D)})/2U_T\right]^2 \ (SI) \end{cases}$ $I_S = 2.n.\beta.U_T^2 \quad U_T \equiv k.T/q$

3. RESULTS AND DISCUSSION

EKV MOSFET model is implemented under matlab m-file (program code), to plot different curves, from detailed model in section 2 (**CONTINUOUS MODEL 'EKV MODEL'**). *Figure 4* and *5* represent the output and transfer characteristics of EKV MOSFET model. *Figures 6* represent the Transconductance g_m as a function of drain current (I_D). *Figures 7* and *8* represent the transconductance efficiency g_m/I_D [11,12] as a function of normalized drain current ($I_D/(W/L)$) and inversion coefficient (I_C), $I_C = I_D/ (I_0\ (W/L))$.

Output and transfer characteristics (*figure 4* and *5*), transconductance *gm* (*figure 6*), transconductance efficiency gm/I_D [11,12] (*figure 7* and *8*) of EKV MOSFET model are important concepts for analog CMOS for the following reasons:

- Method g_m / I_D which allows a rapid initial sizing in all operating regions [18].
- Enable to envisage MOSFET operation over a continuum of inversion levels [13].
- Little touches to make.
- Adopt simple rules for MOSFET sizing in all operating regions [18].
- Relatively reliable calculations: approach a few tens of percent.
- Enable to clearly choose an operating region, which is extremely useful, because each exploitation region possesses distinct characteristics which may or may not be advantageous for a given application.

The results in this work, in good agreement with previous results on Extraction Parameters and electrical characteristic for MOSFETs using various techniques applied to various MOSFETs models [14,15,16,17,19].

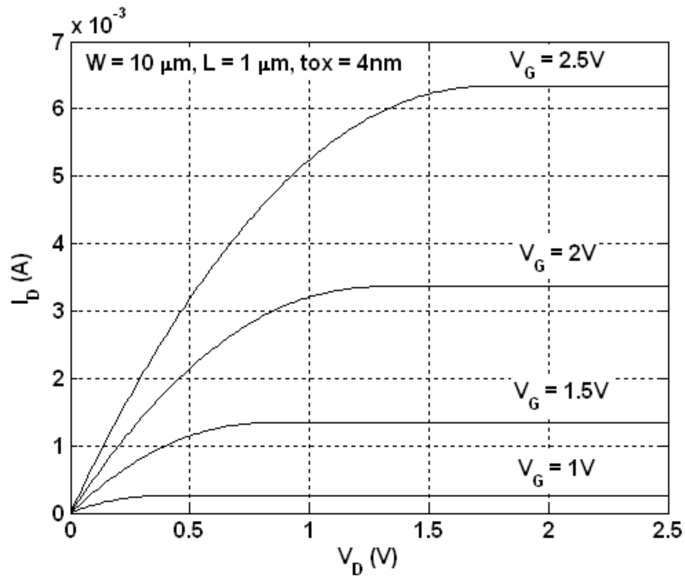

Fig. 4. output characteristics I_D vs. V_D of a short n-channel devices, V_S=0V.

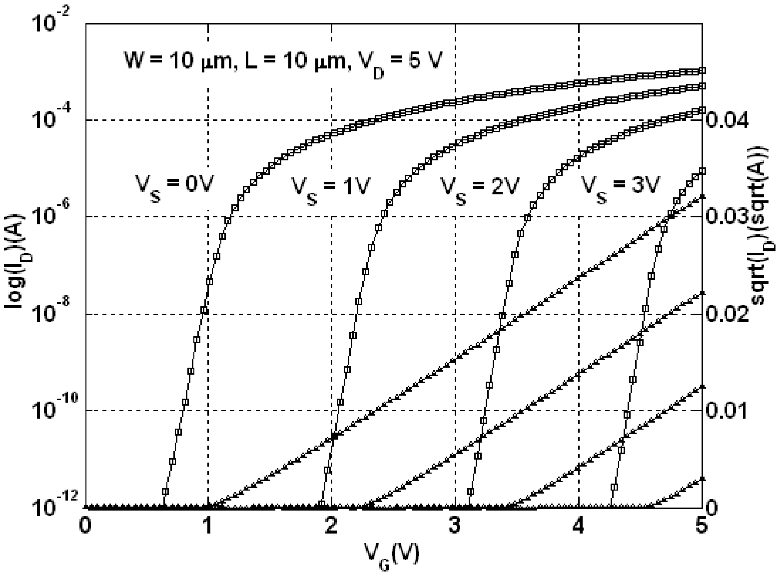

Fig. 5.a) Transfer characteristics log(I_D) & $\sqrt{I_D}$ vs. V_G of n-channel devices, - long-channel

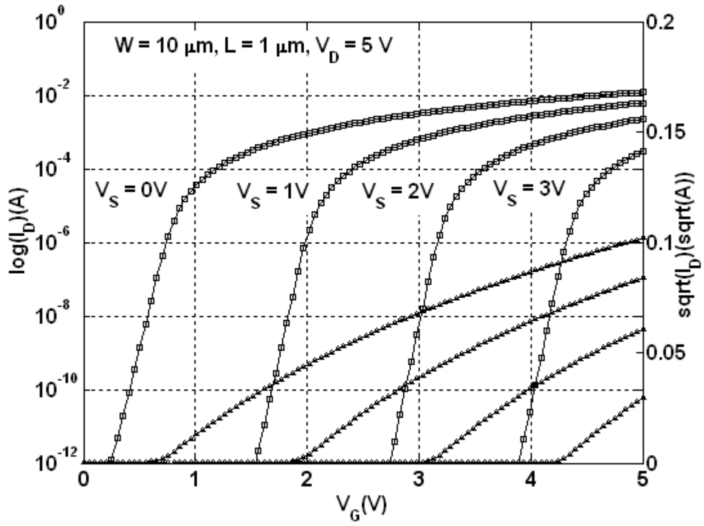

Fig. 5.b) Transfer characteristics log(I_D) & $\sqrt{I_D}$ vs. V_G of n-channel devices, - short-channel.

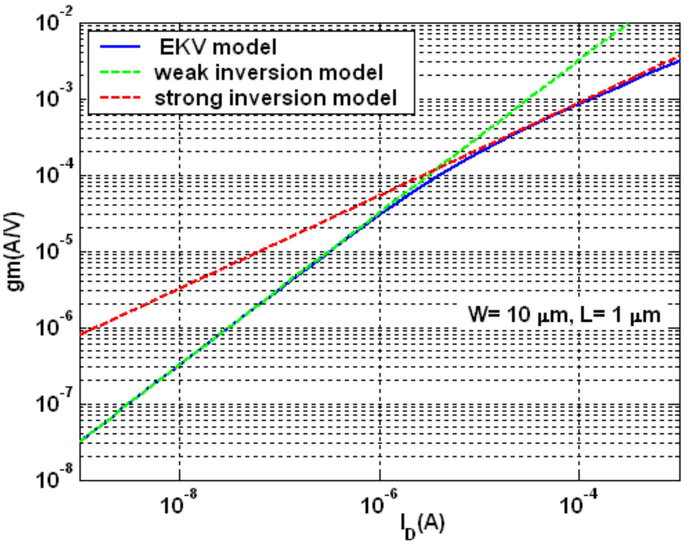

Fig. 6. MOSFET Transconductance gm vs. Drain Current I_D

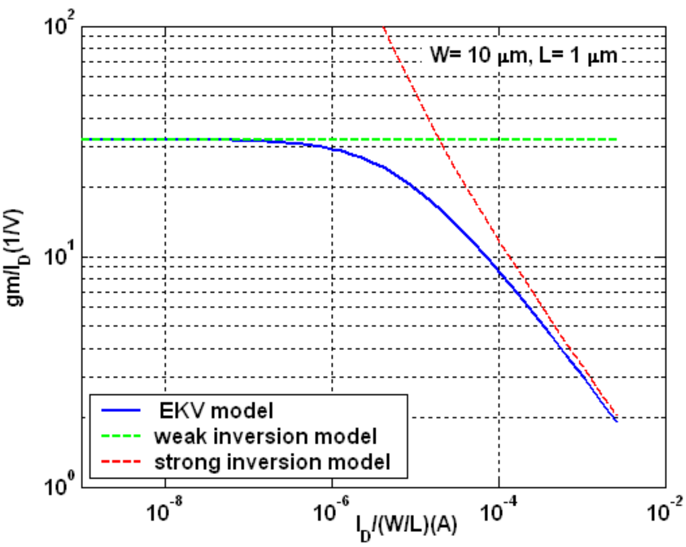

Fig. 7. MOSFET Transconductance Efficiency vs. Normalized Drain Current.

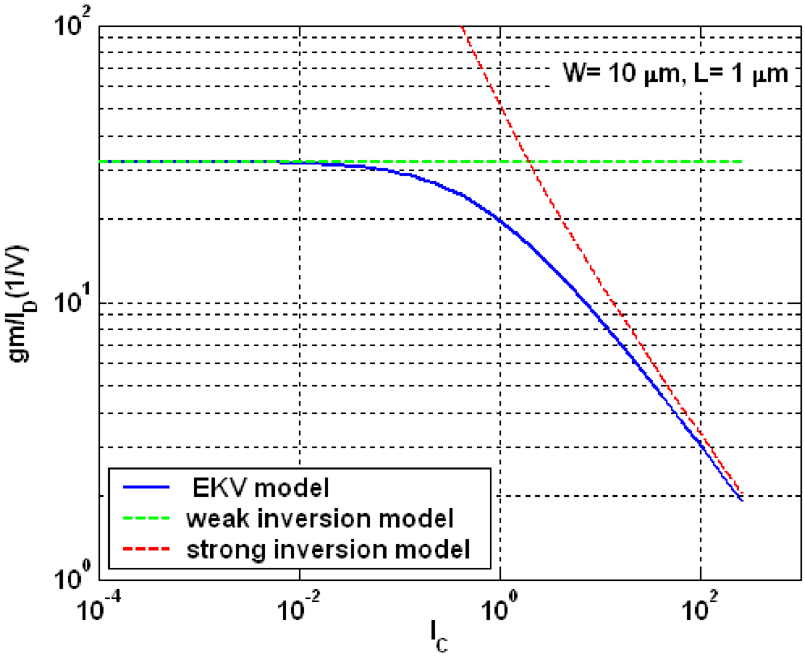

Fig. 8. MOSFET Transconductance Efficiency vs. Inversion Coefficient (I_C).

4. CONCLUSIONS

This paper describes the output and transfer characteristics, the transconductance efficiency, and the transconductances of EKV MOSFET model using Matlab. The EKV model is mathematical model of metal–oxide–semiconductor field-effect transistor (MOSFETs) valid in all regions of operation: weak, moderate, and strong inversion, utilized for circuit simulation and analog circuit design, prepares the path for sizing CMOS circuits suitable for sub-micron low-voltage, low-power circuits. It provides accurate modeling with relates a small signal of parameters to a large signal quantity, does not vary with transistor widths and controls the mode of operation.

REFERENCES

[1] Y. Taur, *CMOS design near the limit of scaling*, IBM Journal of Research and Development, Vol. 46, n°2, pp. 213-220, 2002.

[2] D.J. Frank et al, *Device Scaling Limits of Si MOSFETs and Their Application Dependencies*, Proceedings of the IEEE, Vol. 89, n°3, pp. 259-288, 2001.

[3] D.J. Frank, *Power-constraint CMOS scaling limits*, IBM Journal of Research and Development, Vol. 46, pp. 235-244, 2002.

[4] S. Oda, D. Ferry, *Silicon Nanoelectronics*, Ed. CRC press book, 2005.

[5] J. Wang, M.S. Lundstrom, *Does source-to-drain tunneling limit the ultimate scaling of MOSFET*, Technical Digest. IEEE International Electron Devices Meeting (IEDM), pp. 707-710, 2002.

[6] J.P. Colinge, C.A. Colinge, *Physics of Semiconductor Devices*, Ed. Springer Science -Business Media, 2002.

[7] C. Enz, F. Krummenacher, E.A. Vittoz, *An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low current applications*, Analog integrated circuits and signal processing, Vol. 8, n°1, pp. 83-114, 1995.

[8] C.C. Enz, *The EKV model: a MOST model dedicated to low-current and low voltage analogue circuit design and simulation*, in G.A.S Machado (Ed.), *Low-Power HF Microelectronics: A Unified Approach*, Institution of Electrical Engineers and Technology, pp. 247-300, 1996.

[9] C. Enz, E. Vittoz, *CMOS Low-Power Analog Circuit Design*, Proceeding of IEEE ISCAS, pp. 79-133, 1996.

[10] G.A.S. Machado, C.C. Enz, M. Bucher, *Estimating Key Parameters in the EKV MOST Model for Analogue Design and Simulation*, Proceeding of IEEE International Symposium on Circuits and Systems, pp. 1588-1591, Seattle, Washington, 1995.

[11] F. Silveira, D. Flandre, P.G.A. Jespers, *A gm/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA*, IEEE Journal of Solid-State Circuits, Vol. 31, n°9, pp. 1314-1319, 1996.

[12] W. Rivas-Torres, and Z.S. Roth, *Determination and Study of MOSFET Technology Current*, Canadian Journal on Electrical and Electronics Engineering, Vol. 4, n°2, pp. 75-82, 2013.

[13] D.M. Binkley, M. Bucher, and D.P. Foty, *Design Oriented Characterization of CMOS over the Continuum of Inversion Level and Channel Length*, Proceeding of the 7th International Conference on Electronics, Circuits and Systems (ICECS'2K), pp. 161-164, 2000.

[14] S.C. Terry, J.M. Rochelle, D.M. Binkley, B.J. Blalock, D.P. Foty, M. Bucher, *Comparison of a BSIM3V3 and EKV MOSFET model for a 0.5 um CMOS process and implications for analog circuit design*, IEEE Transactions on Nuclear Science, Vol. 50, n°4, pp. 915-920, 2003.

[15] M. Bucher, C. Lallement, C.C. Enz and F. Krummenacher, *Accurate MOS Modelling for Analog Circuit Simulation Using the EKV Model*, Proceeding of IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 703-706, 1996.

[16] M. Bucher, C. Lallement, C. Enz, F. Theodoloz and F. Krummenacher, *The EPFL-EKV model equations for simulation, v2.6*, Electronics Laboratories, Swiss Federal Institute of Technology, Lausanne (EPFL), 1997.

[17] M. Bucher, C. Lallement and C. Enz, *An efficient parameter extraction methodology for the EKV MOST Model*, Proceeding of IEEE International conference on Microelectronic Test Structures (ICMTS), Vol. 9, pp. 145-50, 1996.

[18] P.G.A. Jespers, *The gm/I_D Methodology, A Sizing Tool for Low-voltage Analog CMOS Circuits*, Ed. Analog circuits and signal processing series, Springer Science+Business Media, 2010.

[19] R.R. Harrison, *MOSFET operation in weak and moderate inversion*, EE 5720, University of Utah.